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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,446	06/30/2001	Balaji Srinivasan	42390P9594	8251

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EXAMINER
MAI, SON LUU

ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/896,446	Applicant(s) SRINIVASAN ET AL.
	Examiner Son L. Mai	Art Unit 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-29* is/are allowed.

6)☒ Claim(s) *1-26 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2-24-03 has been entered. Accordingly, claims 1-33 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 30-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 30, lines 5-6, the recitation "a first drain bias network coupled to the kicker circuit; a second drain bias network coupled to the reference kicker circuit" is misdescriptive. Since the kicker circuit is a part of the first drain bias network, by claiming, "a first drain bias network coupled to the kicker circuit" the Applicants claim the first drain bias network and the kicker circuit are independent elements. Similarly, a correction should be made to the second drain bias network.

Claims 31-33 are rejected for incorporating the limitations of claim 30.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-26 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Jinbo (U.S. Patent 5,305,273).

Regarding claim 1, Jinbo discloses an apparatus comprising: a first drain bias network (14 in fig. 1) having an input suitable to couple to a FLASH cell (MC1); a second drain bias network (15) having an input suitable to couple to a FLASH cell (MCR1); and an equalization circuit (MN13) having a first node (SIN1) coupled to the input of the first drain bias network and having a second node (RIN1) coupled to the input of the second drain bias network and having a control signal (V01) to control operation of the equalization circuit, wherein the equalization circuit is a single equalizing transistor coupled between the first drain bias network and the second drain bias network.

Regarding claim 2, Jinbo's apparatus further comprises: a sense amplifier (16) having a first input (provided with voltage Vsa1), a second input (provided with voltage Vra1), and an output (DAT1); and wherein: the first drain bias network has an output coupled to the first input of the sense amplifier and the second drain bias network has an output coupled to the second input of the sense amplifier.

Regarding claim 3, Jinbo's apparatus further comprises: a reference FLASH cell (MCR1) coupled to the second drain bias network; and a FLASH cell (MC11) coupled to the first drain bias network.

Regarding claim 4, Jinbo also teaches the apparatus comprises: the reference FLASH cell (MCR1) coupled to the second drain bias network (15) through a reference column select transistor (MYR1) and the FLASH cell (MC11) selectively coupled to the first drain bias network (14) through a column select transistor (MY1), the column select transistor controlled by a column select signal (SY1).

Regarding claim 5, Jinbo's figure 1 shows a FLASH cell (MC11) coupled to the first drain bias network (14).

Regarding claim 6, Jinbo's figure 1 shows the FLASH cell (MC11) selectively coupled to the first drain bias network (14) through a first column select transistor (MY1).

Regarding claim 7, Jinbo's figure 1 also shows a reference FLASH cell (MCR1) coupled through a second column select transistor (MYR1) to the second drain bias network (15).

Regarding claims 8 and 9, Jinbo's apparatus further shows the equalization circuit is a transistor (MN13) having a first node coupled to the input (SIN1) of the first drain bias network and having a second node (RIN1) coupled to the input of the second drain bias network and having a control electrode coupled to a third node of the transistor, the control electrode to deliver the control signal (V01).

Regarding claim 10, Jinbo's apparatus further comprises: a reference FLASH cell (MCR1) coupled to the second drain bias network (15).

Regarding claim 11, Jinbo's apparatus shows the reference FLASH cell (MCR1) coupled to the second drain bias network (15) through a reference column select transistor (MYR1).

Regarding claim 12, Jinbo teaches a method comprising: equalizing a sense input and a reference input using a single equalizing transistor (col. 5, lines 35-41); coupling the sense input to a FLASH cell to be sensed (col. 5, lines 12-19); terminating equalization of the sense input and the reference input (col. 5, lines 57-62); and measuring a sense voltage, the sense voltage corresponding to the sense input (col. 5, lines 62-65).

Regarding claim 13, Jinbo also teaches the step of selecting the FLASH cell (col. 5, lines 17-19).

Regarding claim 14, Jinbo also teaches coupling further includes loading the FLASH cell with a load (by load transistor MP11; col. 4, lines 50-54).

Regarding claim 15, Jinbo teaches the method of claim 14 further comprising: coupling the reference input to a reference FLASH cell (col. 5, lines 20-25), including loading the reference FLASH cell (with load transistor MP12); measuring a reference voltage, the reference voltage corresponding to the reference input (col. 5, lines 57-65); and comparing the sense voltage and the reference voltage (col. 5, line 66 through col. 6, line 6).

Regarding claims 16-26, they recite the similar language as claims 1-15. Thus they are rejected as being anticipated by Jinbo.

Regarding claim 30, Jinbo shows in figure 1, an apparatus comprising: a reference cell (MCR1); a kicker circuit (14); a reference kicker circuit (15) coupled to an output of the reference cell; a first drain bias network (MP11) coupled to the kicker circuit; a second drain bias network (MP12) coupled to the reference kicker circuit (15); a sense amplifier (16) with a first input coupled to an output (Vsa1) of the first drain bias network and the sense amplifier with a second input coupled to an output (Vra1) of the second drain bias network; and an equalizing transistor (MN13) coupled between an input of the kicker circuit and an input of the reference kicker circuit.

Allowable Subject Matter

5. Claims 27-29 are allowed.

6. Claims 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the detail limitations of the kicker circuit as claimed in claim 27 or 31 which calls for a kicker circuit including: a first transistor having a first node, a second node and a gate node, the first transistor coupled at its first node to a gate node of a second transistor, to a first node of a third transistor, and to a gate node of a fourth transistor, the first transistor coupled at its second node to ground, and the first transistor coupled at its gate node to a first node of the equalizing

transistor and to a first node of the second transistor the second transistor having a second node, the second transistor coupled at its second node to the first node of the fourth transistor and to the first drain bias network; the third transistor having a second node and a gate node, the third transistor coupled at its second node to a power supply, and the third transistor coupled at its gate node to the power supply; and the fourth transistor having a second node, the fourth transistor coupled at its second node to the power supply.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bashir (U.S. Patent 5,594,691) shows in figure 7, a single equalizing transistor 780 for equalizing potentials at inputs of sense amplifier SA0.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 305-3497. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 308-7724 for regular communications and 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-0956.

03-11-2003

Son Mai
Patent Examiner